IN THE SPECIFICATION:

Please revise paragraph No. [0015] to read as follows:

--[0015] These and other objectives are attained with a method and system for simulating an integrated circuit. The method including the steps of performing a timing analysis of the circuits included in the integrated circuit to ensure that they meet specified timing criteria, performing soft error analysis of the circuits to determine whether they meet specified soft error criteria, and those circuits that fail the soft error analysis to improve their resistance to soft errors. Preferably, the improving step includes the step of improving those circuits that fail the soft error analysis by either having an additional voltage source or altering the capacitance of the circuits.--

Please revise paragraph No. [0025] to read as follows:

--The present invention extends this methodology to include a subsequent filter based on Qcrit analysis. With reference to Figure 4, once timing is done, each path is determined whether it is timing critical based upon a ~~product"s~~ product's frequency goals. If a timing net is deemed non-critical at 32, then the Qcrit net is applied to the net. For nets that are not timing critical, Qcrit can be improved in various ways, as represented by step 44. For example, Vdd can be boosted on the exposed devices, or Qcrit can be raised by adding capacitance or by other circuit techniques that will slow the net down. When a net that is not timing critical is slowed down to fix Qcrit, its timing must be re-evaluated to ensure that it still meets timing requirements.--